TS2GCFX500I **TS16GCFX500I**
TS4GCFX500I **TS32GCFX500I**
TS8GCFX500I

Transcend® good memories start here

Industrial CFast Card

Description

Transcend CFast cards are designed to satisfy high performance requirements using a SATA 3Gb/s interface. As a removable device, it is easier to plug and remove in space-limited applications; such as thin-clients or industrial PCs. Complaint with CFast 1.0 standard, CFast is your best choice as an embedded SATA storage solution."

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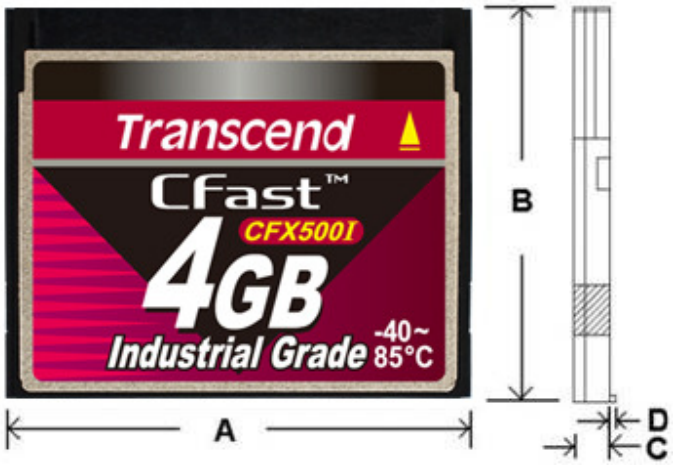
Placement



Features

- RoHS compliant
- CFast Specification Version 1.0 Compliant
- Power Supply: 3.3V±5%
- Operating Temperature: -40°C to 85°C
- Storage Temperature: -40°C to 85°C
- Humidity (Non condensation): 0% to 95%
- Built-in 16bit/30bit per 1KByte ECC (Error Correction Code) functionality ensures highly reliable of data transfer.
- Global wear-leveling algorithm eliminates excessive write operation and extends product life.
- Support S.M.A.R.T (Self-defined)
- Support Security Command
- Fully compatible with devices and OS that support the SATA 3Gb/s standard
- Non-volatile SLC Flash Memory for outstanding data retention
- Durability of Connector: 10,000 times

Dimensions

Side	Millimeters	Inches
A	42.8+/-0.1	1.685+/-0.004
B	36.4+/-0.15	1.433+/-0.006
C	3.3+/-0.1	0.13+/-0.004
D	0.6+/-0.07	0.02+/-0.003

Specifications

Physical Specification		
Form Factor		CFast
Storage Capacities		2GB to 32 GB
Dimensions (mm)	**Length**	42.8 ± 0.1
	Width	36.4 ± 0.15
	Height	3.3 ± 0.1
Input Voltage		3.3V ± 5%
Weight		9.5g
Connector		CFAST connector

Environmental Specifications		
Operating Temperature		- 45 ℃ to 85 ℃
Storage Temperature		- 45 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Reliability		
Data Reliability	Supports BCH ECC 8 bit per 512-byte	
Data Retention	10 years	
Connector Durability	10,000 times	
MTBF	1,000,000 hours	
Endurance (Terabytes Written)	2G	33.68 (TB)
	4G	78.125 (TB)
	8G	160.49 (TB)
	16G	311.29 (TB)
	32G	627.45 (TB)

Regulations	
Compliance	CE, FCC and BSMI

Performance				
Model P/N	**Read**	**Write**	**Random Read**	**Random Write**
TS2GCFX500I	90 MB/s	38 MB/s	13 MB/s	0.1 MB/s
TS4GCFX500I	87 MB/s	73 MB/s	12 MB/s	0.1 MB/s
TS8GCFX500I	107 MB/s	47 MB/s	9.5 MB/s	0.1 MB/s
TS16GCFX500I	115 MB/s	88 MB/s	9.6 MB/s	0.1 MB/s
TS32GCFX500I	112 MB/s	92 MB/s	9.0 MB/s	2 MB/s

Note: 25 ℃, test on ASUS P5Q-PRO, 2GB RAM, Windows® XP Version 2002 SP2 with AHCI mode, benchmark utility Crystal DiskMark (version 3.0), copied file 1000MB, unit MB/s.

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS2GCFX500I	3,865,680	3,835	16	63
TS4GCFX500I	7,732,368	7,671	16	63
TS8GCFX500I	15,465,744	15,343	16	63
TS16GCFX500I	30,932,992	16,383	15	63
TS32GCFX500I	61,865,984	16,383	15	63

Power Requirements		
Input Voltage		3.3V ± 5%
Mode		**Max. (mA)**
TS2GCFX500I	**Write**$_{(peak)}$	219
	Read$_{(peak)}$	237
	Idle$_{(peak)}$	204.5
TS4GCFX500I	**Write**$_{(peak)}$	330
	Read$_{(peak)}$	315
	Idle$_{(peak)}$	228
TS8GCFX500I	**Write**$_{(peak)}$	300.8
	Read$_{(peak)}$	317.5
	Idle$_{(peak)}$	206
TS16GCFX500I	**Write**$_{(peak)}$	348.4
	Read$_{(peak)}$	324.1
	Idle$_{(peak)}$	226.8
TS32GCFX500I	**Write**$_{(peak)}$	368.4
	Read$_{(peak)}$	327.6
	Idle$_{(peak)}$	234.2

Vibration	
Operating	5G(peak to peak), 5 - 800Hz
Non-Operating	20G(peak to peak), 5 - 800Hz

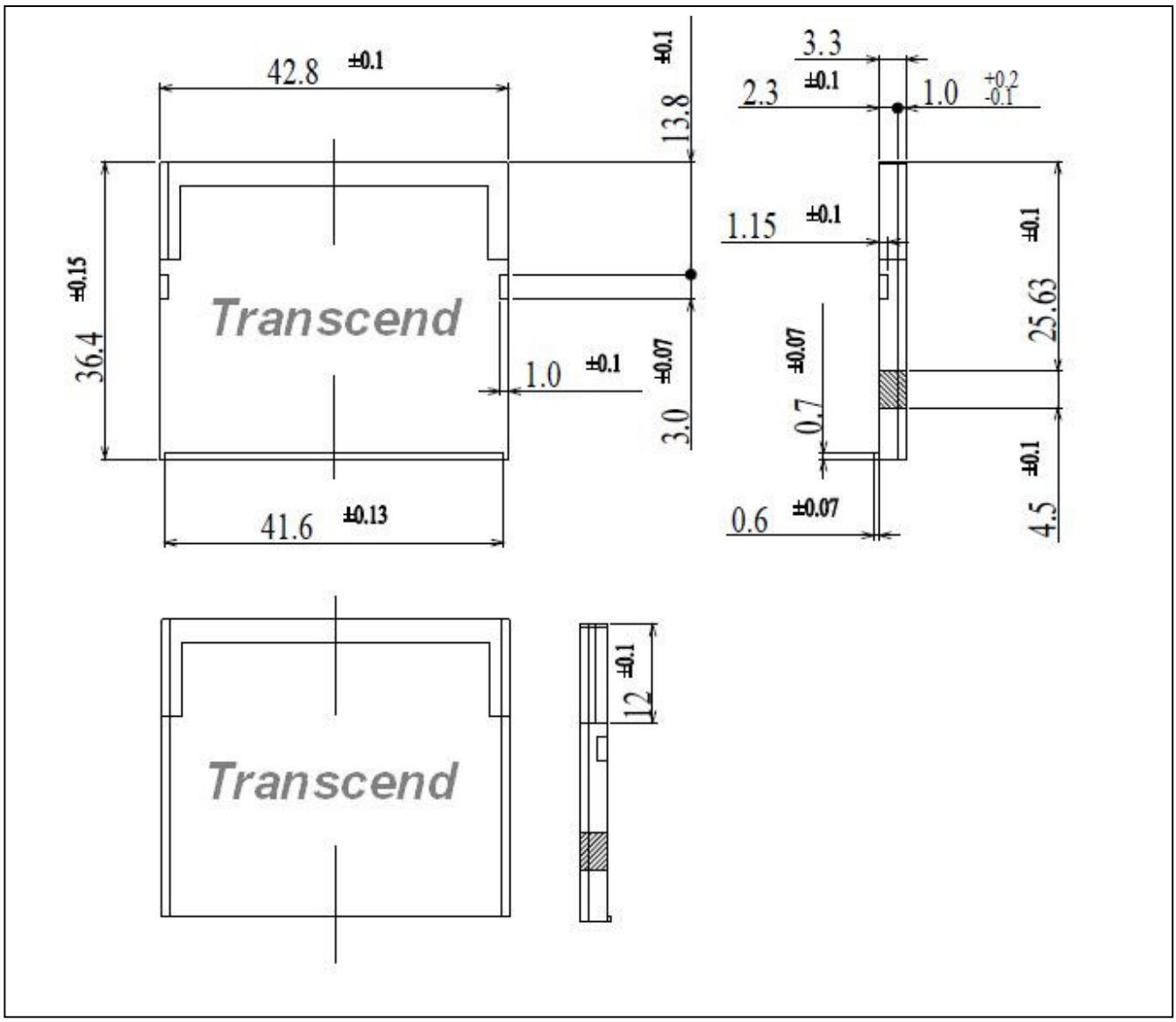
* Reference to IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

* Reference to IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500g, 0.5ms, 3 times/dir., total 18 times.

Package Dimensions

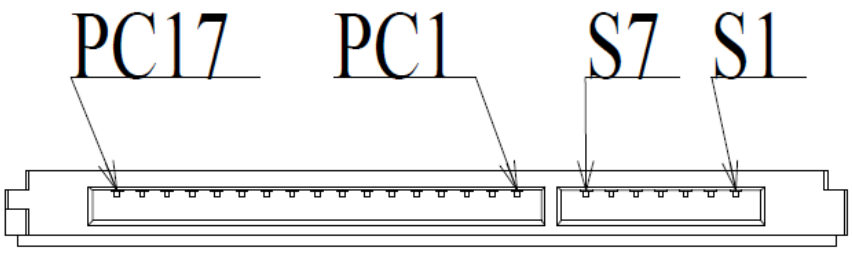
Below figure illustrates the Transcend CFast™. All dimensions are in mm.



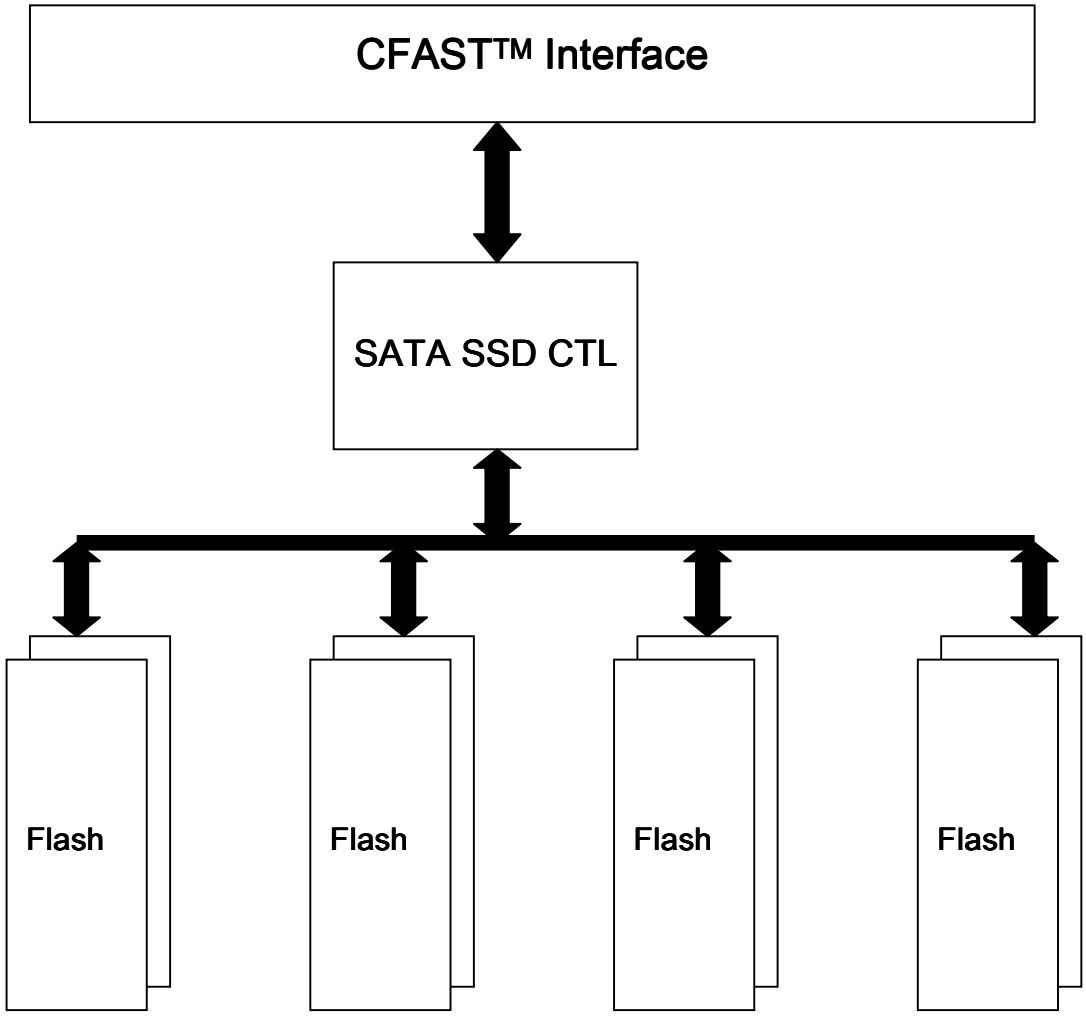
Pin Assignments

Pin No.	Pin Name
7-pin Signal Segment	
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
17-pin Power Segment	
PC1	CDI
PC2	GND
PC3	NC
PC4	NC
PC5	NC
PC6	NC
PC7	GND
PC8	LED_SATA
PC9	LED_DAS
PC10	NC
PC11	NC
PC12	NC
PC13	3.3V
PC14	3.3V
PC15	GND
PC16	GND
PC17	CDO

Pin Layout



Block Diagram



Reliability

Wear-Leveling algorithm

The controller supports static/dynamic wear leveling. When the host writes data, the controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than a threshold value plus data blocks', it will activate the static wear leveling, replacing the not so frequently used user blocks with the high erase count free blocks.

ECC algorithm

Using 1bit BCH Error Correction Code with each channel, the controller can correct 1 random bits per 512 byte data sector for SLC NAND flash. The hardware executes parity generation and error detection/correction features.

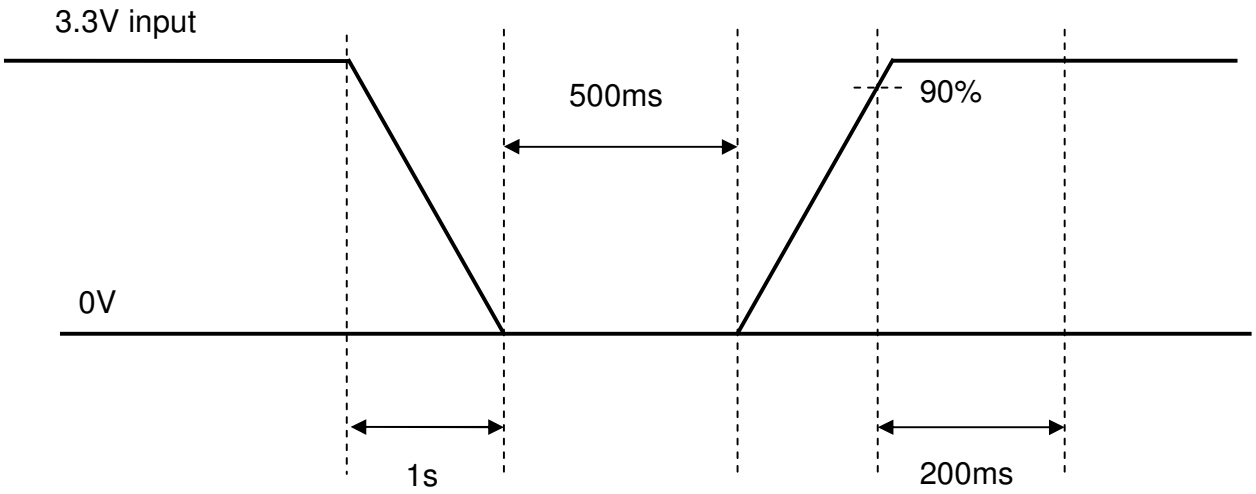
Bad-block management

When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as bad block to prevent the used of this block and caused data lost later on.

Power Sequence

Below figure illustrates the Transcend CFast™ power sequence.

1. Shut down the input power.
2. Power on reset pull low.
3. Wait for the drive to static state.
4. Turn on the input power.
5. Power on to ready pull high.



Measured from 90% VCC to power on to ready

*The actual value may vary depend on device capacity and system environment.

ATA command register

This table with the following paragraphs summarizes the ATA command set.

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
READ DMA	C8h	DMA
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-In
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) EXt	24h	PIO data-In
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-In
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write DMA FUA Ext	3Dh	DMA
Write Multiple Ext	39h	PIO data-out
Write Multiple FUA Ext	CEh	PIO data-out
Write Sector(s) Ext	34h	PIO data-out

ATA Command Specifications

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify "00h" to write 256 sectors.

NOP (00h)

The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the Features register shall not affect the status of any outstanding queue.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data.

WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device's buffer.

Power Management Feature Set

CHECK POWER MODE (E5h or 98h)
The host can use this command to determine the current power management mode.

IDLE (E3h or 97h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h or 95h)
This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

SLEEP (E6h or 99h)
This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

STANDBY (E2h or 96h)
This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h or 94h)
This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

Security Mode Feature Set

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security set Password data content1

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY UNLOCK (F2h)

This command disables LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information

Security Unlock information2

Word	Content		
0	Control word		
	Bit 0	Identifier	0=compare user password 1=compare master password
	Bits 1-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

Identify Device Information Default Value

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Obsolete
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	00XXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer. Supports MDMA Mode 0,1,and 2
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h
66	0078h	2	Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h
67	0078h	2	Minimum PIO transfer cycle time without flow control

Word Address	Default Value	Total Bytes	Data Field Type Information
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-75	0000h	14	Reserved
76	0006h	2	Serial ATA capacities · Support Serial ATA Gen1 · Support Serial ATA Gen2
77-79	000h	6	Reserved
80	0080h	2	Minor version number (ATAPI-7)
81	0000h	2	Minor version number
82	742Bh	2	Command sets supported 0
83	5500h	2	Command sets supported 1
84	4002h	2	Command sets supported 2
85-87	XXXXh	6	Features/command sets enabled
88	407Fh	2	Ultra DMA Mode Supported and Selected
89	0003h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	FFFEh	2	Master Password Revision Code
93-127	0000h	70	Reserved
128	0001h	2	Security status
129-159	0000h	64	Vendor unique bytes
160	0000h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	0000h	2	Reserved
165-175	0000h	22	Reserved
176-255	0000h	140	Reserved

SMART Command Support

Value	Command	Value	Command
D0h	Read Data	D5h	Reserved
D1h	Read Attribute Threshold	D6h	Reserved
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-Line Immediate	DAh	Return Status

If the reserved size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh).

SMART DATA Structure

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-397	F	Number of initial invalid block (396=MSB, 397=LSB)
398-399	V	Number of run time bad block (398=MSB, 399=LSB)
400-406	V	'SMI2242'
407-415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418-419	V	Number of child pair
420	F	Reserved
421-423	V	Average erase count
424-425	V	Number of child pair
426-428	V	Maximum erase count
429-431	V	Minimum erase count
432-445	F	Reserved
446-510	X	Vendor specific
511	V	Data structure checksum

F=the content of the byte is fixed and does not change.

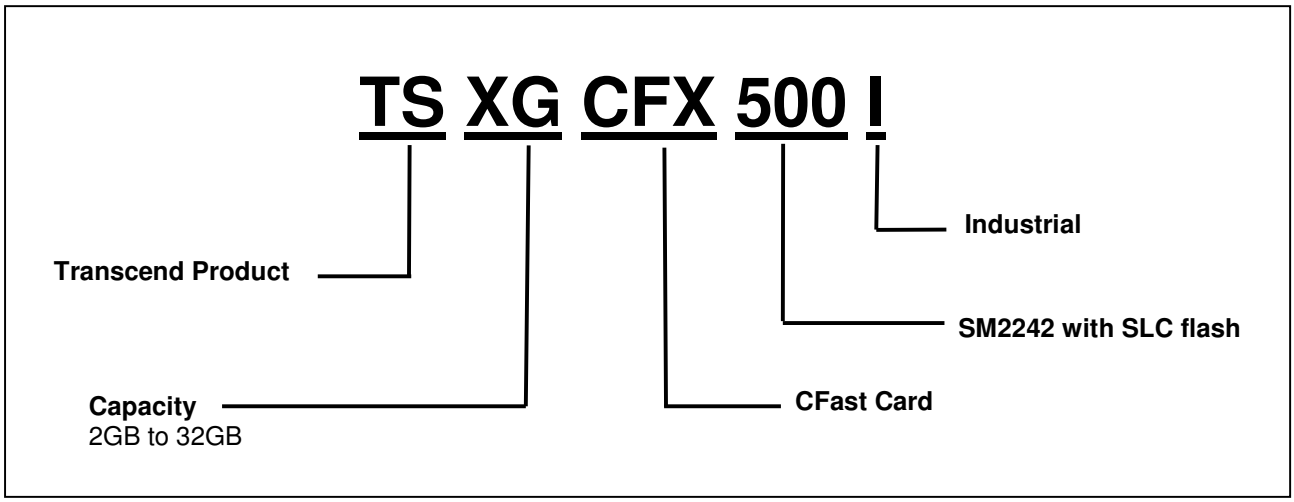
V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X=the content of the byte is vendor specific and may be fixed or variable.

R=the content of the byte is reserved and shall be zero.

* 4 Byte value : [MSB] [2] [1] [LSB]

Ordering Information



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Revision History			
Version	**Date**	**Modification Content**	**Modified Page**
V0.1	2012/06/20	Preliminary	
V0.2	2012/10/3	Add TS2GCFX500I solution	
V0.3	2012/12/14	Modified flash support capability.	1
V1.0	2013/03/08	Modified ATA command related information.	9-17
V1.1	2013/03/29	Add power sequence information	9
V1.2	2013/05/14	Modified pin definition	6