Industrial CFast Card

- CFast Specification Version 1.0 Compliant
- Built-in 16bit/30bit 1KByte ECC (Error Correction Code) functionality ensures highly reliable of data transfer
- Global wear-leveling algorithm eliminate excessive write operation and extends product life.
- Suppot StaticDataRefresh & EarlyRetirement technology to monitor error bit level and react before data is corrupted.
- Fully compatible with devices and OS that support the SATA 3Gb/s standard

CFast Card Benefits

Transcend CFast cards are designed to satisfy high performance requirements using a SATA 3Gb/s interface. As a removable device, it is easier to plug and remove in space-limited applications; such as thin-clients or industrial PCs. Complaint with CFast 1.0 standard, CFast is your best choice as an embedded SATA storage solution. ''

Wear-Leveling algorithm

The controller supports static/dynamic wear leveling. When the host writes data, the controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than a threshold value plus data blocks', it will activate the static wear leveling, replacing the not so frequently used user blocks with the high erase count free blocks.

ECC algorithm

Using 16bit/30bit BCH Error Correction Code with each channel, the controller can correct 16/30bit random bits per 1024 byte data sector for SLC NAND flash. The hardware executes parity generation and error detection/correction

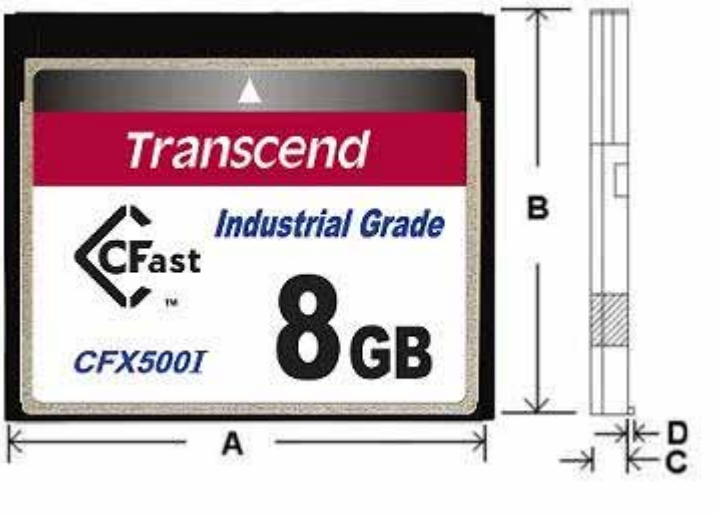
StaticDataRefresh Technology

Normally, ECC engine corrections are taken place without affecting the host normal operations. As time passes by, the number of error bits accumulated in the read transaction exceeds the correcting capability of the ECC engine, resulting in corrupted data being sent to the host. To prevent this, the controller monitors the error bit levels at each read operation; when it reaches the preset threshold value, the controller automatically performs data refresh to “restore” the correct charge levels in the cell. This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data.

EarlyRetirement Technology

The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot reliably store charge anymore, EarlyRetirement enters the scene. EarlyRetirement works by moving the static data to another block (a health block) before the previously used block becomes completely incapable of holding charges for data. When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents its further use, and thus the block enters the state of “EarlyRetirement.”

Placement



Specifications

Environmental Specifications		
Operating Temperature		- 40 ℃ to 85 ℃
Storage Temperature		- 40 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Physical Specification	
Form Factor	CFast
Storage Capacities	2GB~32 GB
Input Voltage	3.3±5%
Weight	9.5g
Connector	CFAST connector

Dimensions

Side	Millimeters	Inches
A	42.8	1.69
B	36.4	1.43
C	3.3	0.13
D	0.6	0.02

Note: Maximum transfer speed recorded

Performance				
Model P/N	**Sequential Read***	**Sequential Write***	**Random Read** (4KB QD32)*	**Random Write** (4KB QD32)*
TS2GCFX500I	90	38	13	0.1
TS4GCFX500I	87	73	12	0.1
TS8GCFX500I	107	47	9.5	0.1
TS16GCFX500I	115	88	9.6	0.1
TS32GCFX500I	112	92	9	2

* 25 ℃, test on ASUS P5Q PRO, 2GB, Windows® XP Professional with AHCI mode, benchmark utility CrystalDiskMark (version 3.0), copied file 1000MB, unit MB/s

* The recorded performance is obtained while the SSD is not operating as an OS disk

Power Requirements		
Input Voltage		3.3V ± 5% @25℃
Mode P/N / Power Consumption		**Typical (mA)**
TS2GCFX500I	$Write_{(peak)}$	219
	$READ_{(peak)}$	237
	$IDLE_{(peak)}$	204.5
TS4GCFX500I	$Write_{(peak)}$	330
	$READ_{(peak)}$	315
	$IDLE_{(peak)}$	228
TS8GCFX500I	$Write_{(peak)}$	300.8
	$READ_{(peak)}$	317.5
	$IDLE_{(peak)}$	206
TS16GCFX500I	$Write_{(peak)}$	348.4
	$READ_{(peak)}$	324.1
	$IDLE_{(peak)}$	226.8
TS32GCFX500I	$Write_{(peak)}$	368.4
	$READ_{(peak)}$	327.6
	$IDLE_{(peak)}$	234.2

Reliability	
Data Reliability	Supports BCH ECC 16 bit/30bit per 1K byte
MTBF	1,000,000 hours

Vibration	
Operating	5G(peak to peak), 5 - 800Hz
Non-Operating	20G(peak to peak), 5 - 800Hz

Note: Reference to the IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms